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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,147	HOBSON, LOUIS B.	
	Examiner	Art Unit	
	Jonathan R. Plante	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the applicant's communication filed 12 July 2007 in response to PTO Office Action mailed 12 April 2007. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

Specification Amendments

2. Acknowledgement of receiving amendments to the specification, which were received by the Office on 12 July 2007. The amendments to the specification included paragraphs 0014, 0024, 0048, 0050, and 0053. The specification has been updated according to reflect amendments.

The objections to the specification have been withdrawn due to amendment filed on 12 July 2007.

Claim Amendments

3. Acknowledgment of receiving amendments to the claims, which were received by the Office on 12 July 2007. Claims 4, 11, 12, 14-16, and 22-24 are amended and there are no new claims.

Claim Amendments 35 USC § 112

4. The 35 U.S.C. § 112-second paragraph rejection of Claim 11 has been withdrawn due to amendments and remarks filed 12 July 2007.

The 35 U.S.C. § 112-second paragraph rejections of Claims 7, 8, 13, 19, and 20 are **NOT** withdrawn due to amendments and remarks filed 12 July 2007.

The Examiner refers Applicant to MPEP § 2173.05(u) "Trademarks or Trade Names in a Claim". Specifically the Examiner refers to:

a. "a trademark or trade name is used to identify a source of goods, and not the goods themselves."

Interpreted, as meaning a trademark or trade name cannot identify a specific product.

b. "If the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982)."

Interpreted, as meaning a trademark or trade name cannot be used as a Claim limitation.

In reference to Claims 7, 8, 13, 19, and 20 Applicant has used either "a Pentium" or "a Pentium 4" trademark as a Claim limitation where Applicant is claiming the physical

embodiment of the "Pentium" or "Pentium 4" processor (e.g. Claim 7, "in a Pentium microprocessor").

Under 35 U.S.C. § 112 second paragraph this is indefinite for both reasons stated above (a, b). First, the "Pentium" and "Pentium 4" trademark can only be used to identify the source of the goods, in this case Intel Corporation. Secondly, Applicant is using "Pentium" and "Pentium 4" as a claim limitation.

Applicant is requested to remove the trademark and trade names from the claims and either cancel the claims or replace them with generic term equivalents.

The Examiner will evaluate these terms using generic term equivalents.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 8, 13, 19, and 20 are rejected under 35 U.S.C. 112, second paragraph, for the presence of trademarks or trade names in the claims. Please see **MPEP 2173.05(u) "Trademarks or Trade Names in a Claim"**.

a. (Claim 7, Line 2) is rejected for the presence of "**TM2 register**" and "**Pentium microprocessor**". The Examiner will evaluate these terms

using generic term equivalents of "a thermal management register" and "a microprocessor".

b. (Claim 8, Line 2) is rejected for the presence of "**PROCHOT**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a control line" and "a microprocessor".

c. (Claim 13, Line 1) is rejected for the presence of "**a Pentium 4 microprocessor**". The Examiner will evaluate this term using generic term equivalent of "a microprocessor".

d. (Claim 19, Line 2) is rejected for the presence of "**TM2 register**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a thermal management register" and "a microprocessor".

e. (Claim 20, Line 2) is rejected for the presence of "**PROCHOT**" and "**Pentium microprocessor**". The Examiner will evaluate these terms using generic term equivalents of "a control line" and "a microprocessor".

Claim Amendments 35 USC § 101

The 35 U.S.C. § 101 rejections of Claims 11 and 22-24 have been withdrawn due to amendments and remarks filed 12 July 2007.

Response to Arguments

7. Applicant's arguments filed 12 July 2007 have been fully considered.

(Claim 1): In response to Applicant's argument associated with "a data structure configured to store an address of a GPIO block" (Remarks, Page 16) the Examiner is not persuaded.

The Examiner refers to:

> the power management module indicates (at 124) the new performance state of the processor is to transition to. This may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor 12. The control register may be defined in memory or I/O address space (Column 12, Lines 39-44)

In view of the above the Examiner notes that the power management module writes a predefined value (e.g. set of bits) to a control register that can be in memory or I/O address space. The Examiner has interpreted an "I/O address space" as being the GPIO block and since the power management module writes the predefined value to the I/O space then the power management module contains/stores an address specifying the specific I/O space to write to.

If Applicant interprets otherwise the Examiner also takes official notice that it would be obvious that the power management module would contain an address since the power management module is writing data to a specific address space or memory. The motivation for the power management module to store and address is so the power

management module can address the data to appropriate I/O address space or memory location in the system.

The Examiner also notes that the power management module is a data structure that can be implemented as a software module, system firmware (e.g. BIOS), or part of the operating system that is stored in memory (Column 12, Lines 29-32).

(Claim 1): In response to Applicant's argument associated with "selecting a bit pattern and writing the bit pattern to the GPIO block" (Remarks, Page 17) the Examiner is not persuaded.

The Examiner refers to:

> the power management module indicates (at 124) the new performance state of the processor is to transition to. This may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor 12. The control register may be defined in memory or I/O address space (Column 12, Lines 39-44)

In view of the above the Examiner notes that the power management module writes a predefined value, indicating the new performance state, to the I/O address space (GPIO block).

The Examiner additionally refers to:

one or more ACPI objects may define the number of performance states available (Column 12, Lines 53-54)

In view of the above the Examiner has interpreted the ACPI objects as being part of the power management module where the ACPI defines multiple performance states (e.g. C1, C2, or C3 state as defined in the ACPI specification (Column 12, Line 60-61)) where the power management module selects a performance state value (bit pattern) and writes it the I/O address space (GPIO block) for indicating a new performance state of the processor.

(Claim 11): In response to Applicant's argument associated with Claim 11 the Examiner is persuaded and a new ground of rejection is presented.

(Claim 14): Examiner has evaluated Method Claim 14 in view of the structure of Claim 1. See Rejection to Claim 14.

(Claims 22 and 23): Are rejected in view of Claim 1.

(Claim 24): In response to Applicant's argument associated with Claim 24 the Examiner is not persuaded. As was noted by the Examine the applicant has only claimed an interface for communicating data between the system components. The applicant has not claimed the ability or application of a user/human interface for interfacing with the system as noted in Applicant Response. The Examiner maintains the 35 USC 102

rejection originally presented, but has also included a 35 USC 103 rejection in view of Applicant's remarks.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-9 and 14-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bhatia et al. (US 6,535,798 B1 March 18, 2003).

Examiner Note: The Examiner will be evaluating the preceding claims in respect to functionality and processes and not by specific boundaries or components. It is ordinary in the art that multiple elements can be functionally separated and contained within multiple elements or contained within a single element or combinations thereof. Examiner refers to Applicant's written description "One of ordinary skill in the art will appreciate that one element may be designed as multiple elements or that multiple elements may be designed as one element. An element shown as an internal component of another element may be implemented as an external component and vice versa. Furthermore, elements may not be drawn to scale" (Page 2, Line 3) and in respect thereto the Examiner will evaluate the prior art.

Examiner Note: The Examiner will be evaluating the following terms in the following way:

a. **GPIO (General Purpose Input Output):** Any functional I/O (Input Output) processor, co-processor, register, computer-readable medium, and/or secondary chip that majority function is I/O routing, multiplexing, and/or switching (e.g. super I/O, bridge chip, I/O circuit, bus chip, router, etc).

b. **Register:** A register as a common term in the art is a storage area for the holding of data for a computer processor the storage area can be but not limited to a latch bank, I/O mapped memory, general memory, and/or system memory. The size of a register is determined by the type of processor, an 8-bit processor will have registers of minimum 8-bits in length, while a 32-bit processors registers are 32-bits in length and so on for 64 and 128-bit processors. At the time of filling March 2004 the general state of the art included 8-bit, 32-bit, and 64 bit processors.

c. **Set of Bits:** It is the Examiners evaluation that a single bit register can contain a bit from a set of bits in respect to the set being [0,1] and a single bit register selecting from the set [0,1] a sub-set of those bits being [0] or [1].

d. **Address:** It is the Examiners evaluation that an address in computer science is a set of bits that describes a specific location within memory (main and/or secondary) that contains data. An address when applicable to computer architecture can define a specific location within memory but

can also define a specific architecture component such as a specific I/O port or system bus. The Examiner will evaluate an "address" in the broadest terms to include both computer architecture and computer science meanings.

e. **Frequency:** It is the Examiners evaluation of both throttling of a clock (stop/start) and increasing and/or decreasing the clock speed are equivalent in terms of the definition for frequency. Frequency as defined as the measurement of the number of times that a repeated event occurs per unit time meaning that throttling and clock speed increasing and/or decreasing are equivalent when evaluated over a period of time. Example: Clock running at 100 cycles per-second (100 Hz) (number of changes/time = frequency) now if the clock runs for only 0.5 seconds and is turn off for 0.5 seconds results in a frequency of only 50 Hz resulting in a frequency change. The 50 Hz frequency can also be achieved by increasing the clock cycle by a factor of 2 resulting in a slower clock that would also decease the frequency to 50 Hz.

(Claims 1 and 22-23): Bhatia et al. discloses, "A system **[COMPUTER SYSTEM (Figure 1, 10)]** for simulating a processor performance state in a processor **["performance states (e.g., cycles the processor between a high and a low performance state)" (ABSTRACT)]**, comprising: a data structure stored in a memory, ***[power management module that is a software module, system firmware, or part of the operating***

system that is stored on memory **(Column 12, Line 29-32)** and **"one or more ACPI objects" (Column 12, Line 46)** ***Where the "ACPI object" is a data structure.***] the data structure being configured to store an address of a GPIO (general purpose input output) block [***The power management module writes a predefined performance state value to a control register or I/O address space (Column 12, Lines 39-44). Where the examiner is equating the I/O address space to a GPIO block and also the power management module contain/storing an address in order to write to the I/O address space (See Response to Arguments)***] and a set of bit patterns [**"ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***The ACPI object has been interpreted to contain multiple entries, equating to a set of entries one entry for each performance state and each performance state would be a specific bit pattern/value.***] that may be written to one or more of, the GPIO block and a thermal management register in the processor, [**"internal control registers in the processor 12 may be used to program the performance state of the processor"(Column 11, Line 8-10)** and **"by writing a predefined value to a control register to indicate the new performance state of the processor 12. The control register may be defined in memory or I/O address space (Column 12, Lines 39-44)]** where the GPIO block is configured to control a thermal management signal that can be provided to the processor, [***The power management module writes the predefined state to the control register for changing the state of the processor where the control register is defined in I/O address space (GPIO block) (Column 12, Lines 39-44)***] and

a logic **["FIG. 7, depicts the "power management control logic" (Column 10, Line 39-51)]** operably connected to the memory, **[*via the* "HOST BRIDGE" (Figure 1, 18), "RAM" (Figure 1, 16)]** the logic configured to receive a request **["SENSOR" (Figure 1, 15)** and **"notification when a sensed temperature rises above a preset target temperature T_t or falls below the target temperature T_t" (Column 3, Line 24-46)]** to establish a desired processor performance state in the processor, **["for controlling the core clock frequency and the supply voltage level of the processor" (Column 10, Line 42)]** to select a bit pattern, the bit pattern being selected from the set of bit patterns, **[*by selecting one of the ACPI activity states the system has selected one state from the set and loaded the appropriate bit set into the register* (Column 11, Line 20-24)]** and to write the bit pattern to the GPIO block or the thermal management register, **[*The power management module writes the bit pattern (predefined value) to the GPIO block (I/O address space)* (Column 12, Line 40-45)]** where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state." **[*The ACPI objects define a number of performance steps by controlling the processor frequency and voltage levels* (Column 12, Lines 53-56)]**.

(Claim 2): In further view of Claim 1, Bhatia et al. discloses, "where the data structure is further configured to store an address of an ACPI status register from which a value related to a frequency and a voltage established in the processor can be read." **[*After the power management module has requested the processor to transition to a***

different state the power management module reads a predefined (know address location/register) in the processor that the processor updates after transitioning (Column 13, Lines 8-14 *and* ***Column 15, Lines 38-45)*****]**

(Claim 3): Bhatia et al. discloses, "where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." **["A non-volatile memory 32 for storing BIOS routines may be located on the bus 46" (Column 3, Line 59-64)** and **"power management module may be implemented as a software module, in system firmware (e.g., system BIOS ...) ... The power management module determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)].**

(Claim 4): Bhatia et al. discloses, "where the data structure comprises an ACPI table **["ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***the ACPI object has been interpreted to consist of a table since the object would contain multiple entries, one entry for each performance state which equates to a table*****]** stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." **[*The ACPI object is part of the power management module which can be "*a software module, in system firmware (e.g., system BIOS"*** ***meaning that the ACPI object is a software data structure stored in system memory or stored directly in the BIOS memory. (Column 12, Line 26-57)*** *and* **"The power management module**

determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)].

Examiner Note: The Examiner additionally refers Applicant to the ACPI Specification that discloses the ACPI table as part of the specification **(1.6 ACPI Specification and the Structure Of ACPI, Advanced Configuration and Power Interface Specification)**. The Examiner also notes that the operating system is contained within the main and/or secondary memory and that the ACPI Specification also discloses communication between the BIOS and OS as part of the ACPI standard **(Figure 1-1 OSPM/ACPI Global System, (Advanced Configuration and Power Interface Specification)**.

(Claims 5): Bhatia et al. discloses, "where the data structure comprises an ACPI table **["ACPI object may define the number of performance states available" (Column 12, Line 53-57)** ***the ACPI object has been interpreted to consist of a table since the object would contain multiple entries, one entry for each performance state which equates to a table***] stored in a Basic Input Output System (BIOS) configured to facilitate controlling a processor function." **[*The ACPI object is part of the power management module which can be* "a software module, in system firmware (e.g., system BIOS" (Column 12, Line 26-57)** ***meaning that the ACPI object is a software data structure stored directly in the BIOS memory.*** *and* **"The power management**

module determines (at 122) if a performance state change is required)" (Column 12, Line 29-35)].

Examiner Note: The ACPI Standard discloses the application of an "ACPI BIOS".

(Claim 6): Bhatia et al. discloses, "where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state." **["more than two performance states may be defined, including a lower performance (LP) state and two higher performance states, referred to as the HP1 and HP2 states" (Column 9, Line 46-49)** and **"Programming the control register ... ACPI objects may define the number of performance states available" (Column 12, Line 44-57)** ***The programming of the control registers is interpreted as loading the "control register" with a specific set of bits correlating to one of the many performance states defined in the "ACPI object".***].

(Claim 7): Bhatia et al. discloses, "where the thermal management register comprises the TM2 register in a Pentium microprocessor." **["internal control registers in the processor 12 may be used to program the performance state of the processor." (Column 11, Line 8-9)** ***Where the Examiner has equated "TM2 register" to "internal control registers" and "Pentium microprocessor" to "processor" replacing trade names/trademarks with equivalent generic terms***].

Examiner Note: See 35 U.S.C. 112 Rejections.

(Claim 8): Bhatia et al. discloses, "where the thermal management signal comprises a signal placed on the PROCHOT line available to a Pentium microprocessor." as **["LO/HI#" Signal (Figure 7)** and **"Processor (Figure 1, 12) T*he Examiner has equated "PROCHOT" to "LO/HI#" signal and "Pentium microprocessor" to "processor" replacing trade names/trademarks with equivalent generic terms*]**.

Examiner Note: See 35 U.S.C. 112 Rejections.

(Claim 9): Bhatia et al. discloses, "the system being incorporated into a computer" as **["COMPUTER SYSTEM" (Figure 1, 10)]**.

(Claim 14): Claim 14 is rejected in view of the structure rejected in Claim 1 and Bhatia et al. disclosing the method with respect to Figure 3: "receiving a request to establish the processor performance state in a processor; **[*Step 304 the temperature exceeds a threshold limit*]** accessing a data store to acquire simulation data that facilitates controlling the a state of a thermal management signal and a thermal management register; **[*Step 306 the processor state is determined by checking the state of the* processor]** and causing the processor performance state to be simulated by causing the processor to change its operating frequency and operating voltage in response to a thermal management signal produced in response to writing a bit pattern to a GPIO block **[*Step 308 if the Processor is in a High Performance state (HP) the processor is transitioned to a Low Performance state (LP).*

(Claim 15): See rejection to Claim 5.

(Claim 16): Bhatia et al. discloses, "where establishing the data structure includes writing a set of bit patterns to the ACPI table **["ACPI objects may define the number of performance states available" (Column 12, Line 53-57)** ***The number of performance states has been evaluated as equating to a number of bit patterns (one pattern for each performance state) and a grouping of a number of individual performance states correlates to a table of performance stats contained in the ACPI object".***] and writing the address of the GPIO block to the ACPI table" **["The location and structure of the control register may be defined under the ACPI object" (Column 12, Line 51)** and **"The control register may be defined in memory or I/O address space" (Column 12, Line 43)** ***When the "control register" is defined in memory the "ACPI object" will contain the memory address (location) for the "control register" so that the "power management module" can write/read the desired bit pattern to the correct memory location. If the "control register" is "I/O address space" (GPIO) then the "ACPI object" will also contain the address so that the "power management module" can write/read the desired bit pattern to the correct "I/O address space" (GPIO).***]

(Claim 17): See rejection to claim 6.

(Claim 18): See rejection to claim 1.

(Claim 19): See rejection to claim 7 and 35 U.S.C. 112 Rejections.

(Claim 20): See rejection to claim 8 and 35 U.S.C. 112 Rejections.

(Claim 21): Bhatia et al. discloses, "acquiring an address of an ACPI status register configured to report a value related to the operating frequency and the operating voltage of the processor;" **[Detection of whether the processor 12 is in the HP or LP state may be accomplished by reading predefined registers in the processor 12 or in other components in the system, including the voltage regulator 52 or the system memory 16. (Column 7, Line 13-17)** and **"The location and structure of the control register may be defined under the ACPI object" (Column 12, Line 51)]** "reading the value from the ACPI status register; and selectively reporting a success or error condition based on the value**. ["After the internal clock frequency and voltage settings have changed, predefined register bits in the processor 12 may be updated that is accessible by software to determine if the performance state change has been successfully made. The predefined register bits may be mapped to a memory or I/O address of the processor 12, the voltage regulator 52, or a combination of both. Alternatively, the predefined register bits may be found in system memory 16." (Column 15, Line 38-45)].**

(Claim 24): Bhatia et al. discloses, "A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling a thermal management signal, comprising: **["The power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above." (Column 12, Line 31)]** a first interface for communicating a bit pattern data; **["the power management module indicates (at 124) the new performance state of the processor is to transition to. This may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor" (Column 12, Line 41)** ***The predefined value is equated to a bit pattern associated with a specific performance state***] a second interface for communicating a GPIO block address data; **["HOST BRIDGE" (Figure 1, 18), "SYSTEM BUS" (Figure 1, 22), "SYSTEM BRIDGE" (Figure 1, 34)**, and **"SECONDARY BUS" (Figure 1, 46)** ***This functional blocks and/or logic blocks transfer data between the processor and non-processor components]]*** and a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a GPIO block identified by the GPIO block address data." **["After the internal clock frequency and voltage settings have changed, predefined register bits in the processor 12 may be updated that is accessible by software to determine if the performance state change has been successfully made. The predefined register bits may be mapped**

to a memory or I/O address of the processor 12, the voltage regulator 52, or a combination of both. Alternatively, the predefined register bits may be found in system memory 16." (Column 15, Line 38-45)].

Examiner Note: The applicant has only claimed an interface for communicating data between the system components. The applicant has not claimed the ability or application of a user/human interface for interfacing with the system as noted in Applicant Response. Examiner additionally cautions Applicant about the addition of new matter, and refers Applicant to the ACPI Specification and the Microsoft's Windows Operating System's power management GUI.

Also see rejections under 35 USC § 103.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (US 6,535,798 B1 March 18, 2003) and general knowledge in the art.**

(Claim 10): It would have been obvious to apply the same system to a printer as applicable to a computer system. Both a computer system and a printer system use microprocessors for processing electrical signals that generate heat and additional electrical components (e.g., power supply, mechanical parts) that also generate heat. Both systems are susceptible to over-heating conditions as a result of the microprocessors and electrical systems being confined within a closed space and as a result both require thermal monitoring and control. Both systems additionally implement mechanical means for discharging excessive heat through the usage of fans and/or vents and also power management associated with on, sleep, and off states.

(Claim 24): In view of the rejection for Claim 24 under 35 USC 102 and if Examiner applies Applicant's interpretation as presented in (Remarks, Page 20) the Examiner rejects Claim 24 under 35 USC 103 as being obvious. Applicant in (Remarks, Page 20) acknowledges that the application and usage of an "API is well understood to provide access to a system to programmers".

Therefore, Claim 24 would have been obvious because the particular technique of suing API's was a know technique and was recognized as part of the ordinary capabilities of one skilled in the art.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (US 6,535,798 B1 March 18, 2003) and Hussain et al. (US 6,172,611 B1 January 9, 2001).

(Claim 11): Bhatia et al. teaches, "A system for simulating a processor performance state in a processor **["A system according to an embodiment of the invention implements a thermal management scheme in which one or more system components are switched between different levels (two or more) of performance states in response to over-temperature conditions or other conditions" (Column 2, Line 24-28)]** that is configured to receive a thermal management signal and to selectively change the processor operating frequency based on the thermal management signal, **["The power management control logic 100, 102 provides control signals to the voltage regulator 52 to adjust its voltage levels and the to the processor 12 to adjust the processor's internal clock frequency." (Column 10, Line 66: Column 11, Line 1-2)]** the system comprising:

a simulation logic configured to produce a simulated thermal management signal; **[*The power management module providing predefined values* (Column 12, Lines 39-42)**

where the predefined values are one or more ACPI performance state values **(Column 12, Line 45-51)]**

a thermal management circuit **["One or more temperature senor units" (Column 3, Line 33-40)]** configured to produce an actual thermal management signal **[*senor units provide sampled temperature T_n* (Column 8, Line 29)]**

However Bhatia et al. fails to explicitly teach "a combination logic configured to selectively provide to the processor one and only one of, the actual thermal management signal and the simulated thermal management signal."

Hussain et al. teaches "a combination logic **["thermal management IC" (Figure 1, 140)]** configured to selectively provide to the processor one and only one of, **[*The thermal management IC provides the ALERT# signal when software thermal thresholds have been exceeded (Column 4, 60-62) and when a hardware thermal threshold has been exceeded provides a shutdown signal OS# (Column 5, Lines 15-18)*]** the actual thermal management signal **["*analog temperature sensor provides to the thermal management IC via connection 135 the system temperature signal (Column 4, Lines 12-21) and hardware controller (Figure 2, 240)*]** and the simulated thermal management signal." **[Software Controller (Figure 2, 230)].**

It would have been obvious to one skilled in the art to combine the teachings of Bhatia et al. with Hussain et al. using the motivation found in Hussain et al. of providing a

critical hardware override circuit in order to shutdown the computer when thermal runaway condition has been encountered to avoid failure or destruction of the electrical components (Column 1, Lines 6-21). Hussain et al. teaches the combination of both software control thermal management with software set points, but also hardware control thermal management with hardware set points that are used in conjunction to regulate the temperature of the CPU. Hussain et al. implements software set points for general thermal management, but retains hardware thermal management for situations when software management has failed or maintain the temperature within set parameters. Hussain et al. also allows the system to be compatible with the ACPI specification while still maintaining the safety and reliability of a hardware thermal management system.

(Claim 12): Is a combination of Claims 1 and 11 and is rejected in view of Claims 1 and 11.

(Claim 13): Hussain et al. teaches the application of using the Pentium or Pentium II microprocessor. It is obvious to one skilled in the art that the technique associated with the Pentium or Pentium II microprocessor was recognized as prior art and was within the capabilities of one skilled in the art to apply to future generations of the Pentium chip family (Pentium 4).

Additionally both Bhatia and Hussain disclose thermal management concerning a processor. The Examiner has equated a "Pentium 4" in generic terms to be a processor.

Conclusion

12. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

When responding to this office action, Applicant is advised that if Applicant traverses an obviousness rejection under 35 U.S.C. 103, a reasoned statement must be included explaining why the Applicant believes the Office has erred substantively as to the factual findings or the conclusion of obviousness See 37 CFR 1.111(b).

Additionally Applicant is further advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday -- Thursday 10:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 6, 2007
JRP

/Jonathan R. Plante/
Examiner, Art Unit 2182

ILWOO PARK
PRIMARY EXAMINER